R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Mai for the indication of allowed claims.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5-8, 10-19 and 21-26 under 35 U.S.C. §102(e) as being anticipated by Choi et al. (U.S. Patent No. 6,381,188; hereinafter Choi) is respectfully traversed and should be withdrawn.

Choi is directed to a dynamic random access memory (DRAM) including a plurality of memory banks and capable of selectively performing self-refresh operation with respect to only a subset of the memory banks (Title and Abstract).

In contrast, the presently claimed invention (claim 1) provides a method for reducing power consumption during background operations in a memory array with a plurality of sections comprising the step of controlling the background operations in each of the plurality of sections of the memory array in response to one or more control signals, where **the background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section**. Claims 10 and 11 include similar limitations.

Choi does not disclose or suggest controlling the background operations in each of the plurality of sections of the

memory array in response to one or more control signals, where **the background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section**, as presently claimed. Therefore, Choi does not disclose or suggest each and every element of a presently claimed invention, arranged as in the present claims as required by MPEP §2131. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, that the refresh bank designating signals PREF_i(i=1 to 4) and the decoding signals PREF_j(j=a' to d') of Choi (see column 9, line 65 through column 10, line 58 of Choi) are similar to the presently claimed one or more control signals and the refresh address signals DRA of Choi are similar to the presently claimed one or more decoded address signals (as suggested on pages 2-3, lines 3-11 of section 3 of the Office Action and for which Applicants' representative does not necessarily agree), Choi does not disclose or suggest that **the background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section**, as presently claimed. In particular, the portion of Choi cited on page 3, lines 1-3 of the Office Action states:

> **If the first refresh bank designating signal PREF_1 is activated, the first decoding signal PREF_a' is activated and the second through fourth decoding signals PREF_b' are deactivated.** ... Thus, the first memory bank 201_1 (FIG. 2) performs a refresh operation and the second through fourth memory banks 201_i (i=2 to 4) do not perform a refresh operation.

> **If the second refresh bank designating signal PREF_2 is activated, the first decoding signal PREF_a' and the second decoding signals PREF_b' are activated and the third and fourth decoding signals PREF_c' and PREF_d' are deactivated**. ... Thus, the first and second memory banks 201_1 and 201_2 perform a refresh operation and the third and fourth memory banks 201_3 and 201_4 do not perform a refresh operation.
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> **If the third refresh bank designating signal PREF_3 is activated, the first through third decoding signals PREF_a', PREF_b' and PREF_c' are activated and the fourth decoding signal PREF_d' is deactivated**. ... Thus, the first through third memory banks 201_1, 201_2 and 201_3 perform a refresh operation and the fourth memory bank 201_4 does not perform a refresh operation.
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> **If the fourth refresh bank designating signal PREF_4 is activated, the first through fourth decoding signals PREF_a', PREF_b', PREF_c' and PREF_d' are all activated.** ... Thus, the first and second [sic; through fourth] memory banks 201_1, 201_2, 201_3 and 201_4 perform a refresh operation (see column 10, lines 15-58 of Choi, emphasis added).

Choi discloses that a refresh operation must occur in memory banks one and two in order for a refresh operation to occur in memory banks three and four (column 10, lines 38-58 of Choi). Since a refresh operation must occur in memory banks one and two when a refresh operation occurs in memory banks three and four, it follows that Choi does not disclose or suggest that the background operations can be enabled simultaneously in two or more of the plurality of sections **independently of any other section**, as presently claimed. Therefore, Choi does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims as required by MPEP §2131. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-9, 12-26, 29 and 30 depend, directly or indirectly, from either claim 1 or claim 11 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 27, 28 and 31 are allowed.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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